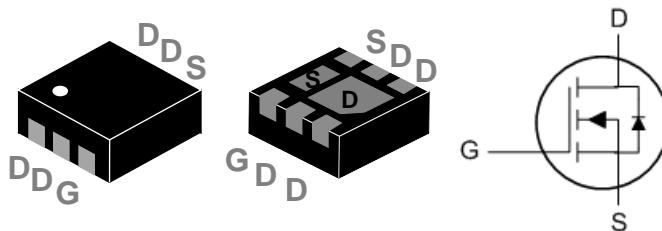


These N-Channel enhancement mode power field effect transistors are using trench DMOS technology. This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency fast switching applications.

DFN2x2-6L Pin Configuration



BVDSS	RDS(ON)	ID
20V	15mΩ	8.5A

Features

20V, 8.5A, RDS(ON) = 15mΩ@VGS = 4.5V

- Improved dv/dt capability
- Fast switching
- Green Device Available
- Suit for -1.8V Gate Drive Applications

Applications

- Notebook
- Load Switch
- Battery Protection
- Hand-held Instruments

Tc=25°C unless otherwise noted

Symbol	Parameter	Rating	Units
V _{DS}	Drain-Source Voltage	20	V
V _{GS}	Gate-Source Voltage	±12	V
I _D	Drain Current – Continuous (Tc=25°C) (Chip Limitation)	8.5	A
	Drain Current – Continuous (Tc=100°C) (Chip Limitation)	6.9	A
I _{DM}	Drain Current – Pulsed ¹ (Chip Limitation)	34	A
P _D	Power Dissipation (Tc=25°C)	2.08	W
	Power Dissipation – Derate above 25°C	0.016	W/°C
T _{STG}	Storage Temperature Range	-55 to 150	°C
T _J	Operating Junction Temperature Range	-55 to 150	°C

Symbol	Parameter	Typ.	Max.	Unit
R _{θJA}	Thermal Resistance Junction to ambient	---	62	°C/W



KRN8A20N

($T_J=25^\circ\text{C}$, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{\text{GS}}=0\text{V}$, $I_D=250\mu\text{A}$	20	---	---	V
$\Delta \text{BV}_{\text{DSS}}/\Delta T_J$	BV_{DSS} Temperature Coefficient	Reference to 25°C , $I_D=1\text{mA}$	---	0.02	---	$\text{V}/^\circ\text{C}$
I_{DSS}	Drain-Source Leakage Current	$V_{\text{DS}}=20\text{V}$, $V_{\text{GS}}=0\text{V}$, $T_J=25^\circ\text{C}$	---	---	1	μA
		$V_{\text{DS}}=16\text{V}$, $V_{\text{GS}}=0\text{V}$, $T_J=125^\circ\text{C}$	---	---	10	μA
I_{GSS}	Gate-Source Leakage Current	$V_{\text{GS}}=\pm 10\text{V}$, $V_{\text{DS}}=0\text{V}$	---	---	± 10	μA

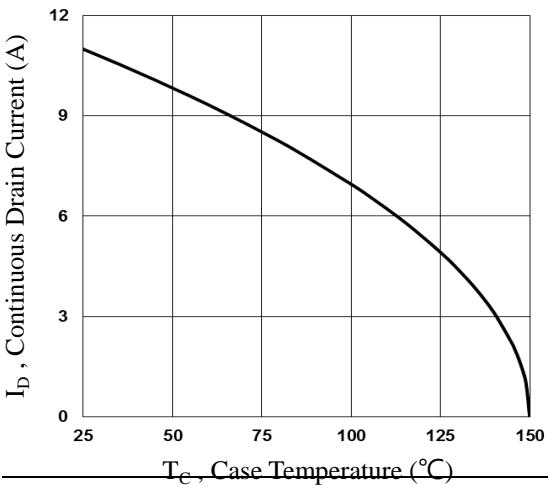
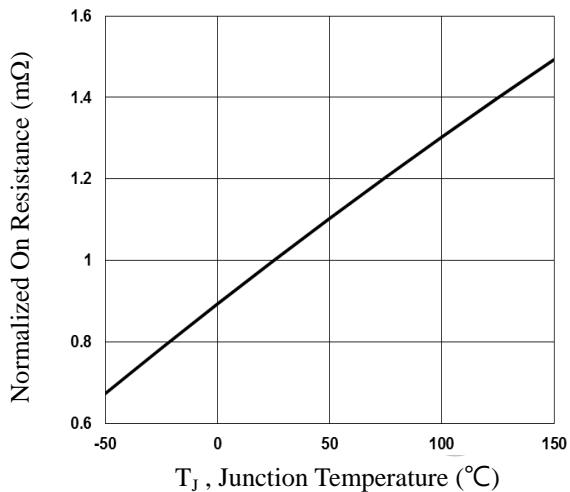
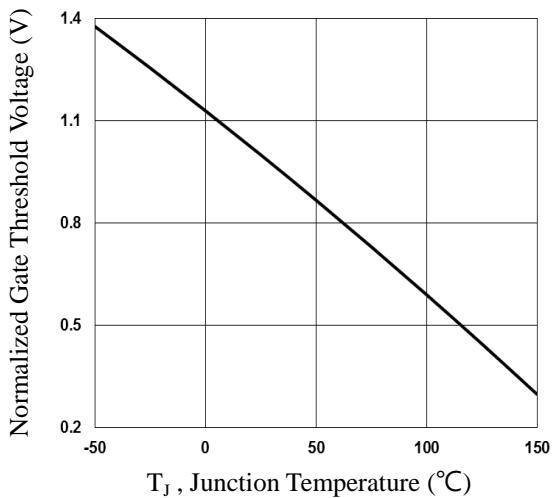
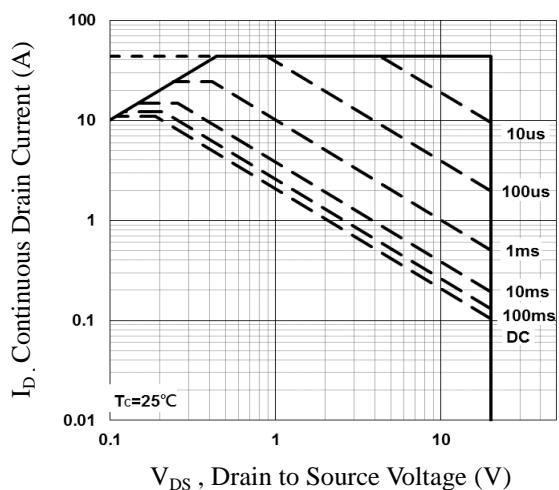
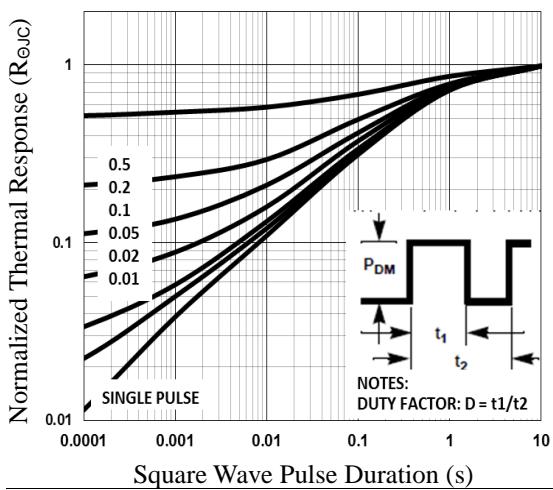
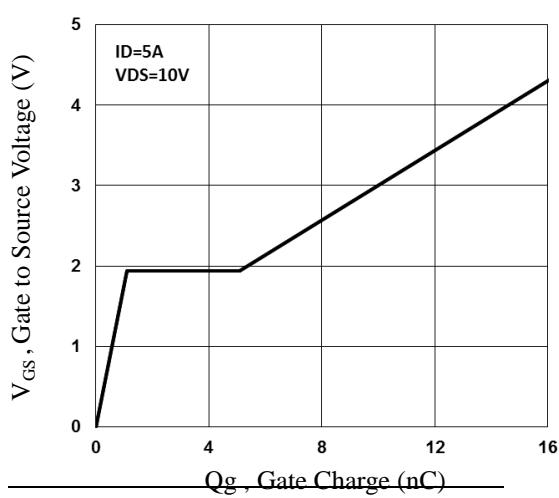
$R_{\text{DS(ON)}}$	Static Drain-Source On-Resistance	$V_{\text{GS}}=4.5\text{V}$, $I_D=5\text{A}$	---	13	15	$\text{m}\Omega$
		$V_{\text{GS}}=2.5\text{V}$, $I_D=3\text{A}$	---	20	23	$\text{m}\Omega$
		$V_{\text{GS}}=1.8\text{V}$, $I_D=2\text{A}$	---	29	37	$\text{m}\Omega$
$V_{\text{GS(th)}}$	Gate Threshold Voltage	$V_{\text{GS}}=V_{\text{DS}}$, $I_D = 250\mu\text{A}$	0.3	0.6	1	V
$\Delta V_{\text{GS(th)}}$	$V_{\text{GS(th)}}$ Temperature Coefficient		---	2	---	$\text{mV}/^\circ\text{C}$
g_{fs}	Forward Transconductance	$V_{\text{DS}}=10\text{V}$, $I_S=5\text{A}$	---	12	---	S

Q_g	Total Gate Charge ^{2,3}	$V_{\text{DS}}=10\text{V}$, $V_{\text{GS}}=4.5\text{V}$, $I_D=5\text{A}$	---	16.9	26	nC
Q_{gs}	Gate-Source Charge ^{2,3}		---	1.1	3	
Q_{gd}	Gate-Drain Charge ^{2,3}		---	4	7	
$T_{\text{d(on)}}$	Turn-On Delay Time ^{2,3}	$V_{\text{DD}}=10\text{V}$, $V_{\text{GS}}=4.5\text{V}$, $R_G=25\Omega$ $I_D=1\text{A}$	---	6.8	13	ns
T_r	Rise Time ^{2,3}		---	20	38	
$T_{\text{d(off)}}$	Turn-Off Delay Time ^{2,3}		---	41.8	79	
T_f	Fall Time ^{2,3}		---	13.2	25	
C_{iss}	Input Capacitance		---	1020	1480	pF
C_{oss}	Output Capacitance	$V_{\text{DS}}=10\text{V}$, $V_{\text{GS}}=0\text{V}$, $F=1\text{MHz}$	---	160	240	
C_{rss}	Reverse Transfer Capacitance		---	110	160	
R_g	Gate resistance	$V_{\text{GS}}=0\text{V}$, $V_{\text{DS}}=0\text{V}$, $F=1\text{MHz}$	---	2	4	Ω

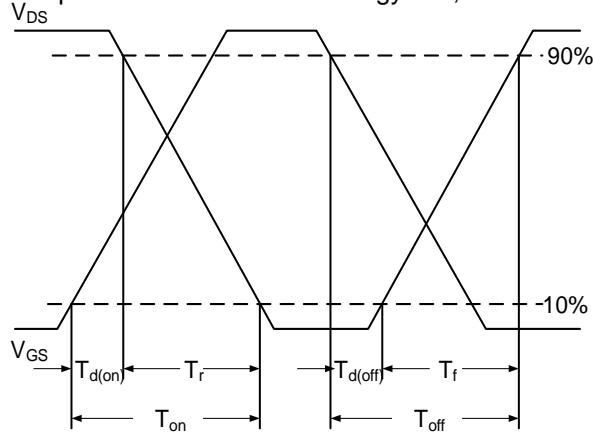
Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_s	Continuous Source Current	$V_G=V_D=0\text{V}$, Force Current	---	---	8.5	A
I_{SM}	Pulsed Source Current		---	---	16	A
V_{SD}	Diode Forward Voltage	$V_{\text{GS}}=0\text{V}$, $I_s=1\text{A}$, $T_J=25^\circ\text{C}$	---	---	1	V

Note :

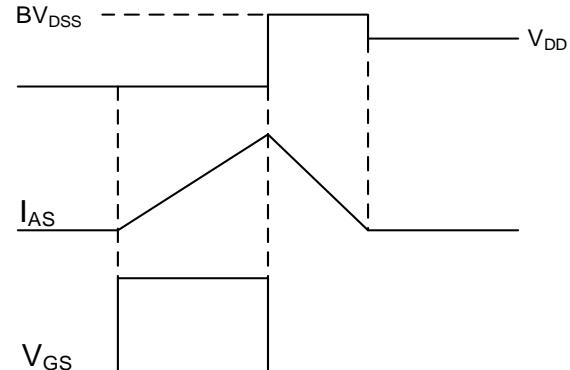
1. Repetitive Rating : Pulsed width limited by maximum junction temperature.
2. The data tested by pulsed , pulse width $\leq 300\mu\text{s}$, duty cycle $\leq 2\%$.
3. Essentially independent of operating temperature.

**Fig.1** Continuous Drain Current vs. T_c **Fig.2** Normalized RD_{SON} vs. T_j **Fig.3** Normalized V_{th} vs. T_j 

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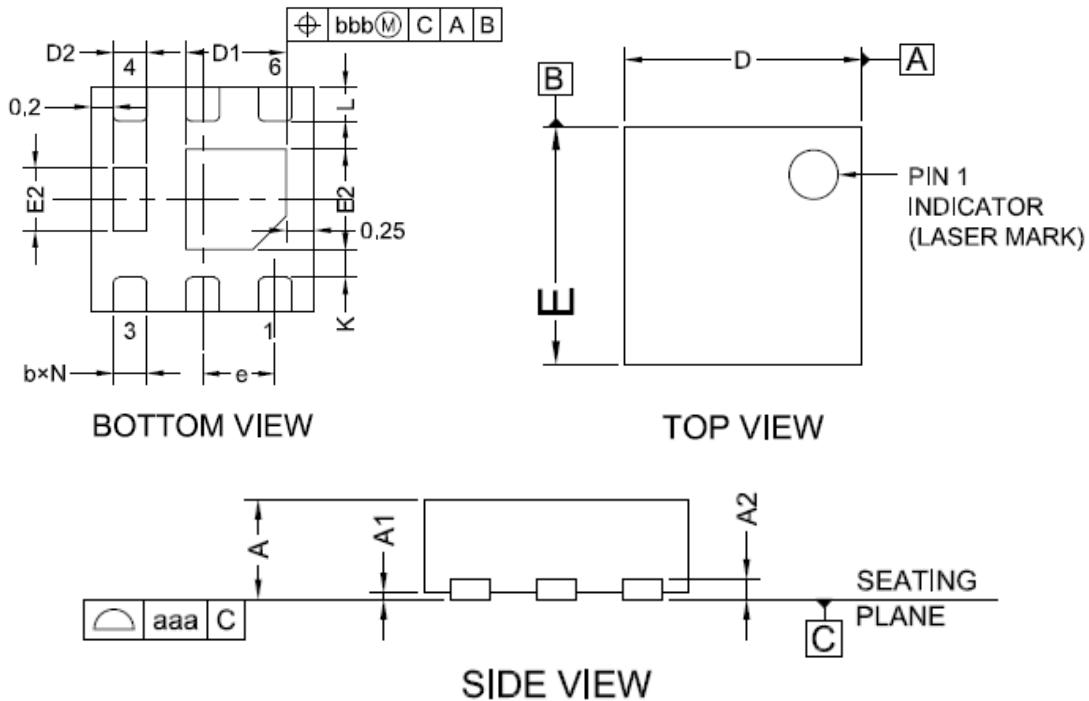


$$EAS = \frac{1}{2} L \times I_{AS}^2 \times \frac{BV_{DSS}}{BV_{DSS}-V_{DD}}$$



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DFN2X2 6L PACKAGE INFORMATION



SYMBOL	MIN	TYP	MAX
A	0.50	0.55	0.60
A1	0.00	0.02	0.05
A2			0.152REF.
b	0.25	0.30	0.35
D	1.95	2.00	2.05
D1	0.80	0.90	1.00
D2	0.25	0.30	0.35
E	1.95	2.00	2.05
E1	0.80	0.90	1.00
E2	0.46	0.56	0.66
e	0.65BSC		
L	0.25	0.30	0.35
J	0.40BSC		
K	0.20MIN		
N	6		
aaa	0.08		
bbb	0.10		